SYSTEM AND METHOD FOR SYNCHRONIZING DIVIDE-BY COUNTERS

Abstract

A synchronization system capable of simultaneously resetting frequency divide-by counters (124_A, 124_B) of multiple processors (A, B) to zero regardless of the divide-by frequency signal (Mclk/n signal (168_A, 168_B)) and regardless of the magnitude of the clock mesh delays experienced by the Mclk/n signals in the processors. The synchronization system includes a mesh delay circuit (176_A, 176_B) for each processor that simulates in the undivided signal (Mclk/1 signal (136_A, 136_B)) the clock mesh delay experienced by the Mclk/n signal in that processor so as to provide an Lclk signal (172_A, 172_B). A phase detector detects the phase offset between the Mclk/n signal and the Sysclk signal (112) and sends an asynchronous offset signal (194_A, 194_B) to a counter re-setter (196_A, 196_B) that resets the divide-by counter to zero based on the offset signal.